



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.                                                                                               | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.    | CONFIRMATION NO. |
|---------------------------------------------------------------------------------------------------------------|-------------|----------------------|------------------------|------------------|
| 10/676,536                                                                                                    | 09/30/2003  | Daniel B. Young      | M-15224 US             | 7660             |
| 7590                                                                                                          | 06/26/2006  |                      | EXAMINER<br>TON, DAVID |                  |
| Jon W. Hallman<br>MacPHERSON KWOK CHEN & HEID LLP<br>Suite 226<br>1762 Technology Drive<br>San Jose, CA 95110 |             |                      | ART UNIT               | PAPER NUMBER     |
|                                                                                                               |             |                      | 2138                   |                  |
| DATE MAILED: 06/26/2006                                                                                       |             |                      |                        |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/676,536

Applicant(s)

YOUNG ET AL.

Examiner

David Ton

Art Unit

2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 9/30/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-10 and 25-27 is/are allowed.
- 6) ☒ Claim(s) 11-14 and 18-24 is/are rejected.
- 7) ☒ Claim(s) 15-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/30/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

1. Claims 1-27 are presented for examination.

***Claim Rejections - 35 USC ' 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 13, 18-19 and 22-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by O'Brien patent no. 6,886,110.

4. As to claim 13, O'Brien disclosed a well known invention as claimed, including a device [see Fig. 5], wherein the device is configurable to form a secondary boundary scan chain [scan chain of device 30'] with a first plurality of boundary scan cells [scan chain of device 30] within at least one external device [device 30'], comprising:

Art Unit: 2138

a second plurality of boundary scan cells [scan cell of device 30'];  
a TDI pin [TDI pin 64];  
a TDO pin [TDO pin 66]; and  
means [bypass register 90 of Fig. 3] for forming a primary boundary scan chain between the TDI pin and the TDO pin including only the second plurality of boundary scan cells and for forming a secondary boundary scan chain between the TDI pin and the TDO pin including the first and the second plurality of boundary scan cells [see col. 6 lines 11-20].

5. As to claim 18, O'Brien teaches the invention as claimed, including a semiconductor device [see Fig. 5], comprising:

a data input pin [pin 64] adapted to receive configuration and/or test data;  
first [pin 62] and second [pin 66] data output pins adapted to transmit configuration and/or test data; and  
a plurality of scan cells forming a scan chain [scan chain of 30, 30' and 30"], wherein the semiconductor device is configurable to couple the scan chain between the data input pin and the first data output pin in a first configuration and to couple the scan chain between the data input pin and the second data output pin in a second configuration [col. 6 lines 11-20].

6. As to claim 19, O'Brien teaches the device include JTAG port [see summary of the invention], TDI pin [TDI of Fig. 5] and TDO pin [TDO of Fig. 5].

7. As to claims 22-24, O'Brien teaches a semiconductor device including a second data input pin adapted to receive configuration and/or test data from a second device, the second data input pin coupled to the first data output pin with the semiconductor device in the second configuration [see Fig. 5 and col. 6 lines 11-20].

***Claim Rejections - 35 USC ' 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 14 and 20-21 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over O'Brien patent no. 6,886,110.

10. As to claim 14, O'Brien does not teach a configuration memory cell wherein the state of the configuration memory cell controlling whether the primary or the secondary scan chain is formed (or bypass).

Official Notice is taken that using a state of a configuration memory cell for controlling circuit is well known in the art.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to substitute the bypass register taught by O'Brien by using a configuration memory cell wherein the state of the configuration memory cell controlling whether the primary or the secondary scan chain is bypassing as a matter of design choice. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a circuit easy for controlling through the state of the memory cell.

11. As to claims 20-21, O'Brien does not teach the device is a programmable logic device or a programmable power supply sequence controller.

Official Notice is taken that a programmable logic device or a programmable power supply sequence controller is well known in the art.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to apply the JTAG test circuit taught by O'Brien into a programmable logic device or a programmable power supply sequence controller for testing these device. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a convenient and shorten the time it take to test multiple device using boundary scan [see O'Brien col. 6 lines 11-20].

12. Claims 11-12 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over O'Brien patent no. 6,886,110 in view of Crouch et al. (Crouch) patent no. 5,592,493.

13. As to claims 11-12, O'Brien teaches the claimed invention substantially as shown in claims 13 and 18 above. However, O'Brien does not teach the bypass circuit is implement by a demultiplexer and a multiplexer.

Crouch teaches an analogous art [see Fig. 2] by using a DEMUX 40 and a MUX 24 to bypass the scan chain 70-84, 104-112 or 124-138 in device 32, 34 or 36 [see col. 9 lines 20-53].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to implement the bypass circuit taught by O'Brien using a MUX and DEMUX components as taught by Crouch as a matter of design choice. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a simple bypass circuit as taught by Crouch.

#### ***Allowable Subject Matter***

14. Claims 1-10 and 25-27 are allowed.

15. Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

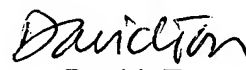
#### ***Conclusion***

16. The prior art of record and not relied upon is considered pertinent to applicant's disclosure.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
David Ton  
Primary Examiner  
Art Unit 2138